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First Named Inventor	James M. Derderian
Art Unit	2811
Examiner Name	J. Im
Attorney Docket Number	2269-4832US (01-0104.00/US)

ENCLOSURES ***(check all that apply)***

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☒ Reply Brief
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
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- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
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- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
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Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 AND 1.17 TO Deposit Account 20-1469 during pendency of this application.

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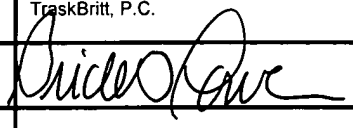
Signature			
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: James M. Derderian

Serial No.: 09/938,106

Filed: August 23, 2001

For: ASSEMBLIES INCLUDING STACKED SEMICONDUCTOR DEVICES SEPARATED BY DISCRETE CONDUCTIVE ELEMENTS THEREBETWEEN, PACKAGES INCLUDING THE ASSEMBLIES, AND METHODS

Confirmation No.: 1038

Examiner: J. Im

Group Art Unit: 2811

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REPLY BRIEF

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Attn: Board of Patent Appeals and Interferences

Sirs:

This Reply Brief follows the Examiner's Answer of December 15, 2006, and is being filed pursuant to 37 C.F.R. § 41.41.

VII. ARGUMENT

A. REJECTIONS UNDER 35 U.S.C. § 102

1. APPLICABLE LAW

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

With respect to inherency, M.P.E.P. § 2112 provides:

> The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish inherency of that result or characteristic. *In re Rijckaert,* 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) . . . 'To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill . . .'' *In re Robertson,* 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1991) (emphasis supplied).

2. REFERENCE RELIED UPON

Wu

Wu discloses a stacked semiconductor structure and a method of manufacturing such a structure that, in part, protects the wires of a semiconductor die from contact that die in the assembly. Col. 2, lines 44-47; Col. 3, lines 37-41, 54-56. Wu provides a substrate 26 that includes signal input terminals 40 and a projecting element 52, or dam, formed on the periphery of the substrate 26. Col. 3, lines 1-3, 21-22; FIGs. 3-5. A glue layer 30 is used to adhere a lower semiconductor chip 28 to the substrate 26, the semiconductor chip 28 pressing the glue 30 from

underneath the lower surface 44 of the semiconductor chip 28 towards the periphery of the substrate 26. Col. 3, lines 15-20, FIG. 3. The projecting element 52 prevents the glue layer 30 from spreading across the substrate 26 and forces it to flow up and over a portion of the periphery of the upper surface 46 of the semiconductor chip 28. Col. 3, lines 19-26; FIG. 3. After the semiconductor chip 28 is adhered to the substrate 26, bond wires 32 are connected to bond pads 48 on the upper surface 46 of the semiconductor chip 28 and the signal input terminals 40 on the substrate 26, the bond wires 32 located over the overflow glue that covers a portion of the periphery of the upper surface 46 of the semiconductor chip 28. Col. 3, lines 29-38; FIG. 3. The adhered glue 50 on the upper surface 46 of the semiconductor chip 28 prevents the bond wires 32 from contacting the semiconductor chip 28. Col. 3, line 40-41; FIGs. 3-4. Element 54, undefined in the specification, but labeled in the drawings, appears between the bond pads 48.

An upper semiconductor chip 34 is "stacked above lower semiconductor chip 28 *by adhered glue* 50." Col. 3, lines 39-40; FIG. 3 (emphasis added). While not stated in the specification, it appears that element 54 also supports the upper semiconductor chip 34. *See* FIG. 4. The bond wires 32 are pressed, or *pinched*, between the upper semiconductor chip 34 and the glue 50 that overlies the periphery of the upper surface 46 of the lower semiconductor chip 28. Col. 3, lines 54-56; FIGs. 4-5. Bond wires 56 connect the upper semiconductor chip 34 to the signal input terminals 40 of the substrate 26. Col. 3, lines 41-43; FIG. 4. A package layer 58 is subsequently applied to cover the substrate 26, lower semiconductor chip 28, and upper semiconductor chip 34.

3. ANALYSIS

Claims 23, 24, 29, 30, 33, 40, 45, 46, 49, 50, 53, 59, and 61-64 have been rejected under 35 U.S.C. § 102(e) for reciting subject matter which is purportedly anticipated by that described in Wu.

It is apparent that the Examiner did not focus on the subject matter recited in claims 23, 24, 29, 30, 33, 40, 45, 46, 49, 50, 53, 59, and 61-64. Instead, it appears that the Examiner focused on the subject matter disclosed in the specification of the above-referenced application.

Independent claim 23 recites, among other things, "positioning a second semiconductor device at least partially over [a] first semiconductor device, a back side of the second semiconductor device *resting upon at least some . . . discrete conductive elements and being supported thereby . . .*" (emphasis supplied). Independent claim 45 recites, among other things, "positioning a second semiconductor device at least partially over [a] first semiconductor device and on at least some discrete conductive elements . . . such that *the second semiconductor device is supported by the at least some discrete conductive elements . . .*"

It has been asserted, at pages 2 and 3 of the Final Office Action of April 5, 2005 that FIG. 5 of Wu shows wires 32 supporting the second semiconductor die 34. The figures of Wu can only be relied upon for what they reasonably show, based on the specification of Wu. M.P.E.P. § 2125. For a drawing to constitute an enabling disclosure a picture must show all the claimed structural features and how they are put together. *Jockmus v. Leviton*, 28 F.2d 812 (2d Cir. 1928); M.P.E.P. § 2121.04. Figure 4 of Wu does not clearly depict any of the features located between the first semiconductor die 28 and the second semiconductor die 34. Moreover, the figures of Wu could not be considered to definitively show that the wires 32, rather than

some other features, such as element 54 or the adhered glue 50, supports the second semiconductor die 34. The broadest reasonable interpretation one skilled in the art would reach, in view of the specification that expressly states that the "upper semiconductor chip 34 is stacked above lower semiconductor chip 28 by adhered glue 50" and FIGs. 3-4, is that the element 54 and the glue 50 support semiconductor chip 34, rather than the strained interpretation that the delicate bonding wires 32 pressed, or pinched, between the glue 50 and the upper semiconductor chip 34 support the semiconductor chip 34. Col. 3, lines 38-40, lines 54-56; FIGs. 3-5; *In re Wright*, 569 F.2d 1124, 193 USPQ 332 (C.C.P.A. 1977); M.P.E.P. § 2125.

Each of claims 24, 29, 30, 33, and 40 is allowable, among other reasons, for depending either directly or indirectly from claim 23, which is allowable.

Claim 30 is additionally allowable since Wu does not expressly or inherently describe "drawing" second semiconductor chip 34 toward first semiconductor chip 28. Instead, the description of Wu is limited to "stack[ing]" second semiconductor chip 34 above first semiconductor die 28. Col. 3, lines 37-40; FIG. 4. As evidenced by the disclosures of U.S. Patents 4,891,436 and 6,156,146, resins and other adhesive materials do not necessarily shrink when cured. They may instead expand. Furthermore, Wu is silent as to whether adhered glue 50 is in a cured or uncured state when second semiconductor die 34 is positioned over adhered glue 50. As adhered glue 50 does not necessarily shrink when cured and since adhered glue 50 is not necessarily in an uncured state when second semiconductor chip 34 is positioned above the first semiconductor chip 28, Wu does not inherently describe each and every element of claim 30. *See In re Rijckaert*, 9 F.3d 1531, 1534 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990); M.P.E.P. § 2112 (IV).

Claim 33 is also allowable since Wu includes no express or inherent description that a quantity of adhesive material (adhered glue 50 or element 54) is applied to an active surface of first semiconductor die 28 "after . . . positioning the second semiconductor" die 34 thereover. Instead, Wu clearly discloses that adhered glue 50 is applied to first semiconductor die 28 before second semiconductor die 34 is positioned thereover. Col. 3, lines 36-40.

Each of claims 46, 49, 50, 53, 59, and 61-64 is allowable, among other reasons, for depending either directly or indirectly from claim 45, which is allowable.

Claim 50 is additionally allowable since Wu does not expressly or inherently describe "drawing" second semiconductor die 34 thereof toward first semiconductor die 28, as discussed above vis-à-vis claim 30.

Claim 53 is also allowable since Wu includes no express or inherent description that a quantity of adhesive material (adhered glue 50 or element 54) is applied to an active surface of first semiconductor die 28 "after . . . positioning the second semiconductor" die 34 thereover, as discussed above vis-à-vis claim 33. Instead, Wu clearly discloses that adhered glue 50 is applied to first semiconductor die 28 before second semiconductor die 34 is positioned thereover. Col. 3, lines 36-40.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 23, 24, 29, 30, 33, 40, 45, 46, 49, 50, 53, 59, and 61-64 be reversed.

B. REJECTIONS UNDER 35 U.S.C. § 103(a)

1. APPLICABLE LAW

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

2. ADDITIONAL REFERENCE RELIED UPON

Lee

Lee teaches a process for forming a multi-chip module. That process includes, among other things, adhering a first semiconductor chip 21 to a substrate 30 with an adhesive layer 28. Col. 5, lines 5-7; FIG. 1. Through a reverse wiring bonding process, bond wires 22 are made to connect bond pads 210 on semiconductor chip 21 to the substrate 20. Col. 5, lines 8-21; FIG. 1.

After the bond wires 22 are connected, an electrically insulative adhesive layer 23 is applied over the first semiconductor chip 21. Col. 5, lines 22-25; FIG. 1. The adhesive layer 23 envelops the portions of the bond wires 22 that are located over the first semiconductor chip 21 so that the bond wires 22 are protected during the process of mounting the second semiconductor chip 24 over the first semiconductor chip 21. Col. 5, lines 25-32; Col. 5, lines 53-59 (bond

wires 22 are "*entirely buried*" in the adhesive layer 23) (emphasis added); FIG. 1. Thus, the adhesive layer 23 supports the second semiconductor chip 24 to ensure the quality of the process used to connect the bond pads 240 of the second semiconductor chip 24 to the bond pads 220 on the substrate 20 with bond wires 25. Col. 6, lines 1-13.

3. ANALYSIS

a. WU IN VIEW OF LEE

Claims 25, 26, 31, 34, 35, 41-44, 47, 51, 54-58, and 60 have been rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over the subject matter taught in Wu, in view of teachings from U.S. Patent 6,388,313 to Lee, *et al.* (hereinafter "Lee").

Claims 25, 26, 31, 34, 35, and 41-44 are each allowable, among other reasons, for depending indirectly from claim 23, which is allowable.

Each of claims 47, 51, 54-58, and 60 is allowable, among other reasons, for depending indirectly from claim 45, which is allowable.

i. NO MOTIVATION TO COMBINE

It is also respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 25, 26, 31, 34, 35, 41-44, 47, 51, 54-58, or 60 because one of ordinary skill in the art would not have been motivated to combine the teachings of Wu and Lee in the manner that has been asserted. As discussed above, Wu does not teach or suggest that delicate bond wires support an overlying semiconductor chip, a deficiency that Lee does not

remedy. As Lee sets forth, it is the adhesive layer 23 that supports the overlying semiconductor chip, rather than the bond wires that are *entirely buried* in the adhesive. Col. 5, lines 53-59; Col. 6, lines 1-13; FIG. 1.

Rather, it appears that an impermissible reliance upon the subject matter recited in the claims and disclosed in the specification of the above-referenced application have provided th Examiner with the alleged motivation to combine teachings from Wu and Lee. Thus, one skilled in the art wouldn't have been motivated to combine the teachings of Wu with those of Lee in the manner that the Examiner has asserted.

ii. NO EXPECTATION OF SUCCESS

It is further submitted that one of ordinary skill in the art would have had no reason to expect the asserted combination of teachings from Wu and Lee to be successful. Indeed, as discussed above and as Lee makes clear, it is the adhesive layer that supports the overlying semiconductor chip, which does not remedy Wu's previously discussed deficiencies.

iii. THE REFERENCES DO NOT TEACH OR SUGGEST EACH AND EVERY ELEMENT OF SEVERAL CLAIMS

It is further submitted that Wu and Lee, taken either together or separately, do not teach or suggest each and every element of several of the rejected claims, as is required to establish a *prima facie* case of obviousness.

Claim 31, which depends from claim 30, is allowable since Wu and Lee both lack any teaching or suggestion that the adhesive materials or resins disclosed therein are capable of drawing two semiconductor devices toward one another "by at least one of capillary action . . ., curing . . ., application of heat . . . , and vibration." While Wu and Lee both teach use of adhesive layers to secure adjacent elements, neither Wu nor Lee teaches or suggests an adhesive layer that is capable of drawing two elements toward one another, as discussed above vis-à-vis claim 30, from which claim 31 depends.

Claim 34 is allowable because neither Wu nor Lee teaches or suggests that two semiconductor device may be drawn toward one another for the reasons set forth in claims 30 and 31, among others.

Claim 35, which depends from claim 34, is also allowable since Wu and Lee do not teach or suggest that curing of a glue, resin, or other adhesive material may cause two semiconductor devices to be drawn toward one another.

Claim 51, which depends from claim 50, is allowable since both Wu and Lee lack any teaching or suggestion that the adhesive materials or resins disclosed therein are capable of drawing two semiconductor devices toward one another "by at least one of capillary action . . ., curing . . ., application of heat . . . , and vibration." While Wu and Lee both teach use of adhesive layers to secure adjacent elements, neither Wu nor Lee teaches or suggests an adhesive layer that is capable of drawing two elements toward one another, as discussed above vis-à-vis claim 50, from which claim 51 depends.

Claim 54 is allowable because neither Wu nor Lee teaches or suggests that two semiconductor device may be drawn toward one another for the reasons set forth in claims 50 and 51, among others.

Claim 55, which depends from claim 54, is also allowable since Wu and Lee do not teach or suggest that curing of a glue, resin, or other adhesive material may cause two semiconductor devices to be drawn toward one another.

Claim 57 is allowable because Wu and Lee both lack any teaching or suggestion of controlling biasing of one semiconductor device toward another.

Claim 58 is allowable since neither Wu nor Lee includes any teaching or suggestion of "controlling biasing force to a level insufficient to deform, kink, bend, or collapse . . . discrete conductive elements." Lee teaches that the adhesive layer 23 entirely buries the bond wires 22, which prevents the wires 22 from being damaged during the mounting of the second semiconductor chip 24 onto the first semiconductor chip 21. Lee, Col. 5, lines 55-59. Wu teaches the use of a projecting element 52 and overflow glue 50 to prevent shorting of wires 32 against first semiconductor die 28 as second semiconductor die 34 presses wires 32. Wu, Col. 3, lines 50-62. Thus, neither Wu nor Lee teaches or suggests a method that includes controlling a biasing force.

b. WU IN VIEW OF SHIM

Claims 27, 32, and 48 are rejected under 35 U.S.C. § 103(a) for being directed to subject matter that is assertedly unpatentable over the teachings of Wu, in view of teachings from U.S. Patent 6,531,784 to Shim, *et al.* (hereinafter "Shim").

Claims 27 and 32 are both allowable, among other reasons, for depending indirectly from claim 23, which is allowable.

Claim 48 is allowable, among other reasons, for depending indirectly from claim 45, which is allowable.

Reversal of the 35 U.S.C. § 103(a) rejections of claims 25-27, 31, 32, 34, 35, 41-44, 47, 48, 51, 54-58, and 60 is respectfully requested.

C. ELECTION OF SPECIES REQUIREMENT

It is respectfully submitted that independent claims 23 and 45 remains generic to all of the species of invention of the second group that was identified in the Election of Species Requirement in the above-referenced application. In view of the allowability of these claims, claims 36-39 and 52, which have been withdrawn from consideration, should also be considered and allowed. M.P.E.P. § 806.04(d).

II. CONCLUSION

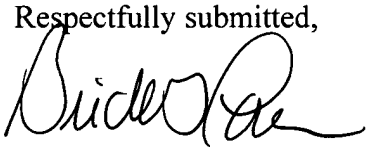
(A) The subject matter recited in claims 23, 24, 29, 30, 33, 40, 45, 46, 49, 50, 53, 59, and 61-64 is novel and, thus, under 35 U.S.C. § 102(e), patentable over the subject matter described in Wu;

(B) Claims 25, 26, 31, 34, 35, 41-44, 47, 51, 54-58, and 60 are drawn to subject matter that is non-obvious and, thus, under 35 U.S.C. § 103(a), patentable over the subject matter taught in Wu, in view of teachings from Lee; and

(C) Under 35 U.S.C. § 103(a), the subject matter to which claims 27, 32, and 48 are directed is allowable over the teachings of Wu, in view of teachings from Shim.

Therefore, the rejections of claims 23-27, 29-35, 40-51, and 53-64 should be reversed. Additionally, claims 36-39 and 52 should be returned to consideration, and each of claims 23-27 and 29-64 should be allowed.

Respectfully submitted,



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